# AN ANALYTICAL MODEL FOR HARDENED LATCH SELECTION AND EXPLORATION

NVIDIA

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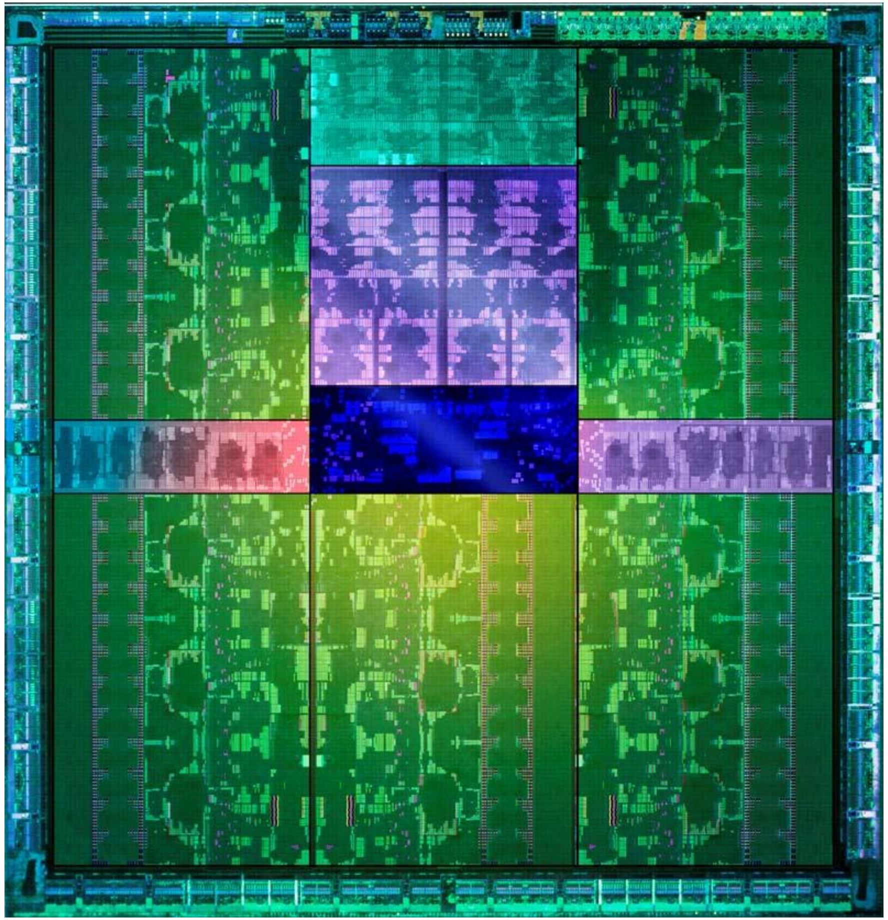
# CHIP USE AND OVERVIEW



Logic: Low Priority

SRAMs/Latch Arrays/Busses: ECC

Unstructured Flip-Flops:
Need Protection

# FLIP-FLOP HARDENING

Will always be unstructured flip-flops (ECC ineffective)

Flip-Flop Hardening:

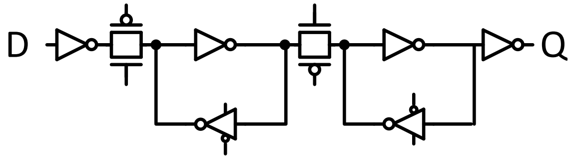
- Avoid errors in certain flip-flops
- Goal: unobtrusive yet effective way to reach FIT targets

Want to understand how hardening affects system level resiliency

- **Which flip-flops to harden? How to harden them? The overall impact?**

# TYPES OF HARDENING

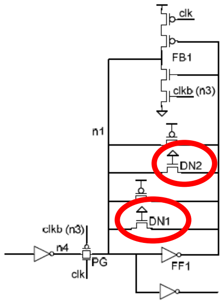
## ① Existing Flip-Flops




Different
- Area
- Power
- Timing

FIT differences

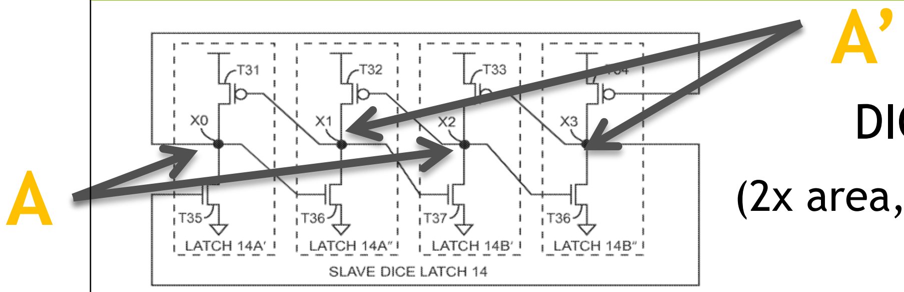
## ② Strike Suppression




RCC

(1.15x area, 6x FIT)

## ③ Redundant Node



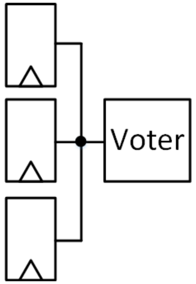

DICE

(2x area, 40x FIT)

## ④ Triple Modular Redundancy

TMR

(3.5x area, 1,000,000x FIT)



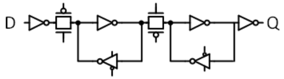
# MANY TYPES OF HARDENING

RCC: Reinforcing Charge Collection
(Seifert 2010 IRPS)

BISER: Built-In Soft Error Resilience
(Zhang 2006 IEEE Trans. VLSI)

RTS: Reverse TriState
(Seifert 2012 IEEE Trans. Nuclear Science)

① Existing Flip-Flops




Different
- Area
- Power
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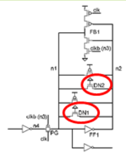
FIT differences

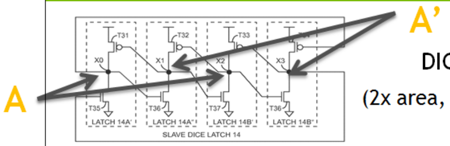
② Strike Suppression



RCC
(1.15x area, 6x FIT)

DICE: Dual-Interlocked Storage Cell
(Calin 1996 IEEE Trans. Nuclear Science)

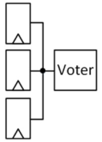
③ Redundant Node




DICE
(2x area, 40x FIT)

④ Triple Modular Redundancy

TMR
(3.5x area, 1,000,000x FIT)




LEAP: Layout Design through Error-Aware Transistor Positioning
(Lee 2010 IRPS)

Quatro: Soft Error Robust Flip-Flops
(Jagannathan 2011 IEEE Trans. Nuclear Science)

SEUT: Single-Event Upset Tolerant
(Seifert 2012 IEEE Trans. Nuclear Science)

LEAPDICE
(Lilja 2013 IEEE Trans. Nuclear Science)

# EXAMPLE HARDENED FLIP-FLOP CHOICES

| Flip-flop type | Area overhead | Power overhead | FIT reduction |
|---|---|---|---|
| Baseline | 1x | 1x | 1x |
| Strike suppression technique | 1.15x | 1.15x | 6x |
| Redundant node | 2x | 2x | 40x |
| Triple-modular-redundancy (TMR) | 3.5x | 3.5x | 100,000,000x |

# HARDENING UNCERTAINTY

Validation requires a tape-out and beam testing

- Only approximate improvement known before tape-out

Beam testing results have uncertainty---experimental variation and low error counts

Literature evaluations differ

- Neutron, proton, heavy ion beams
- Clock and input pattern methodology
- Temperature, voltage, process corner

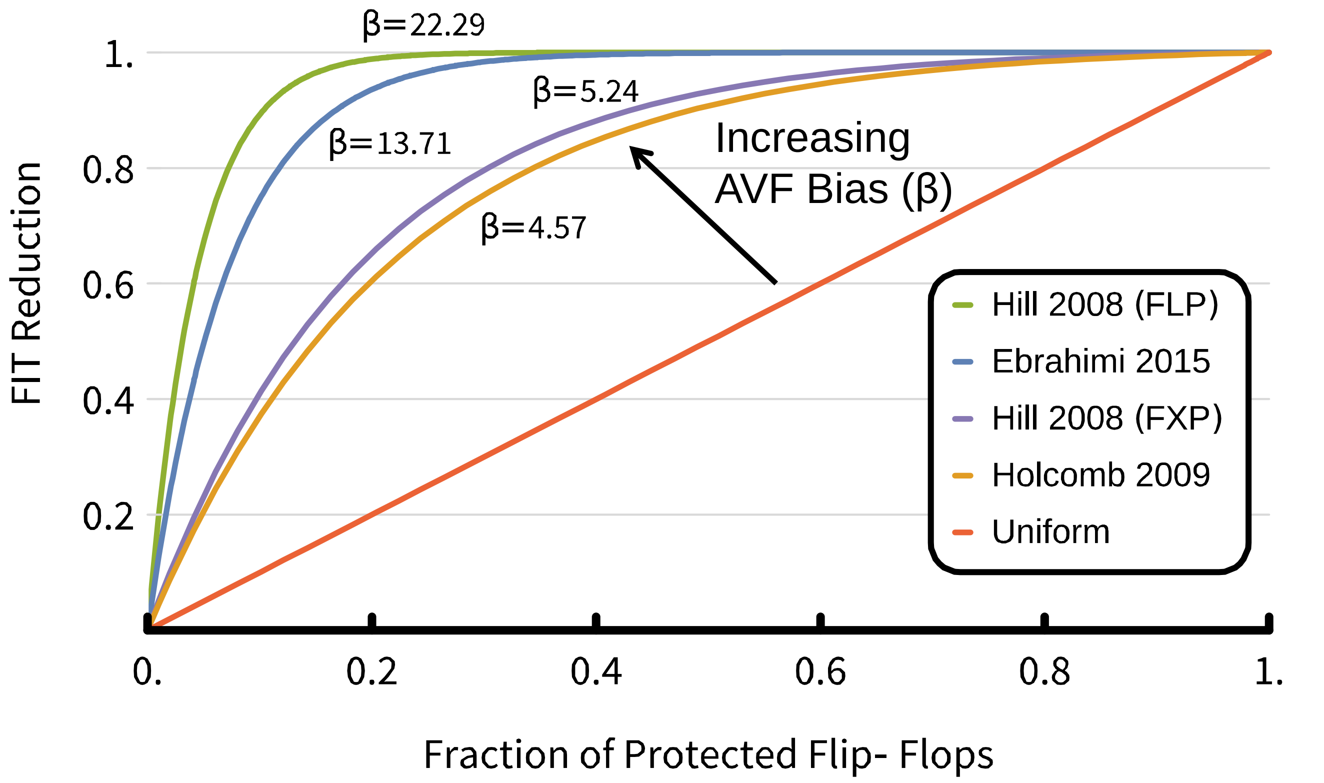
Need a transparent model for sensitivity and uncertainty sweeps

# ANALYTICAL MODEL

## Goals

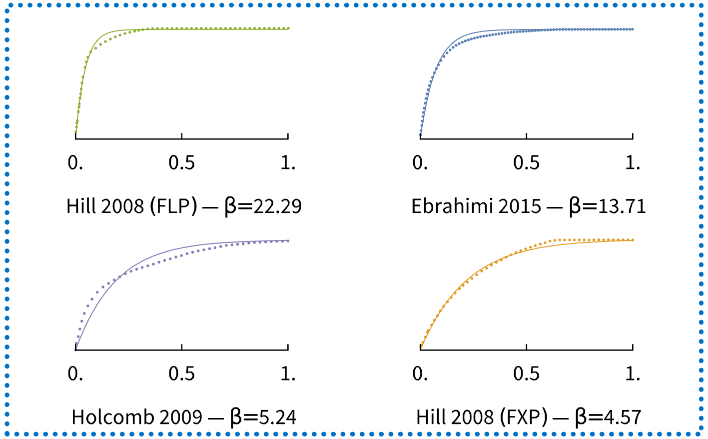
1. Capture the asymmetric sensitivity of flip-flops
2. Express differing flip-flop protection levels and costs
3. Simplicity and transparency

# CHARACTERIZING FLIP-FLOP SENSITIVITY

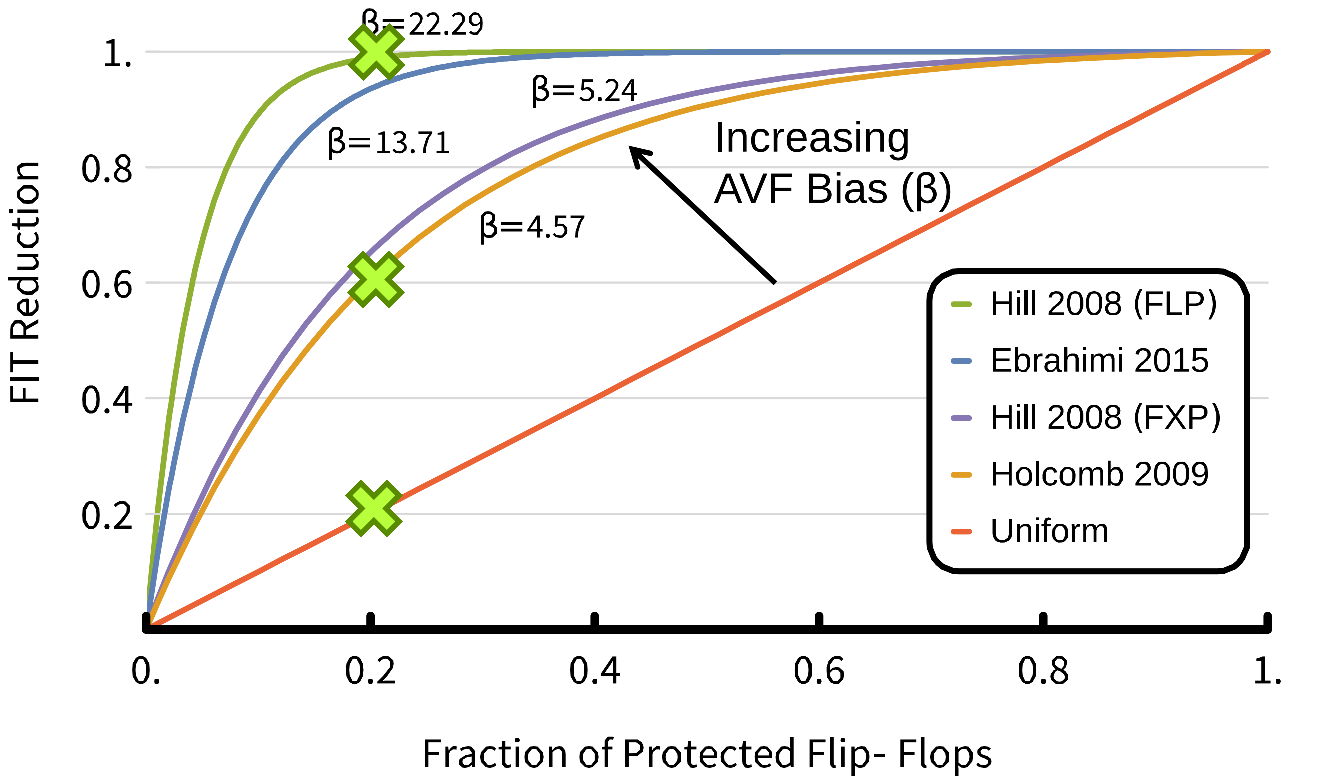



β = Flip-flop AVF Bias

Empirically Fit to Data



# THE IMPACT OF ASYMMETRIC SENSITIVITY



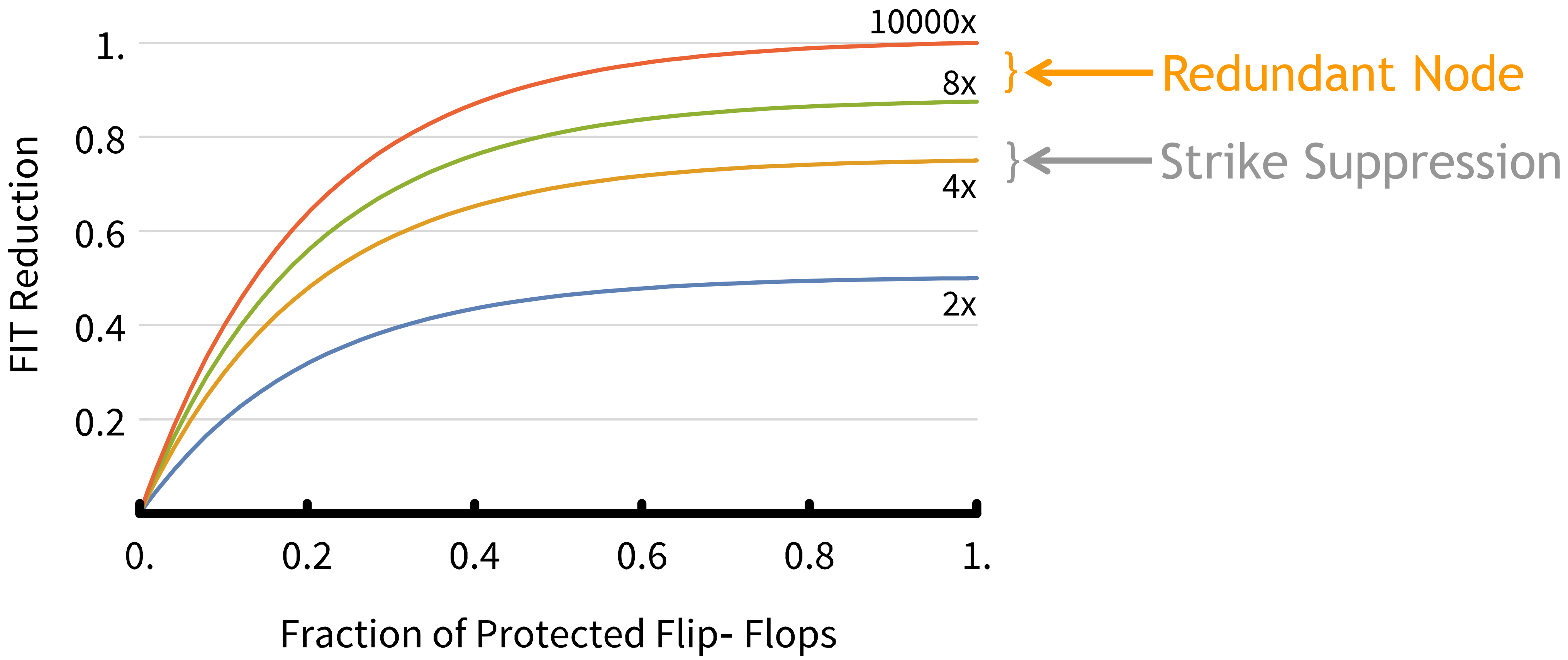

Hardening 20% FFs:

Hill 2008 FLP (β = 22.29):
98.8% FIT reduction

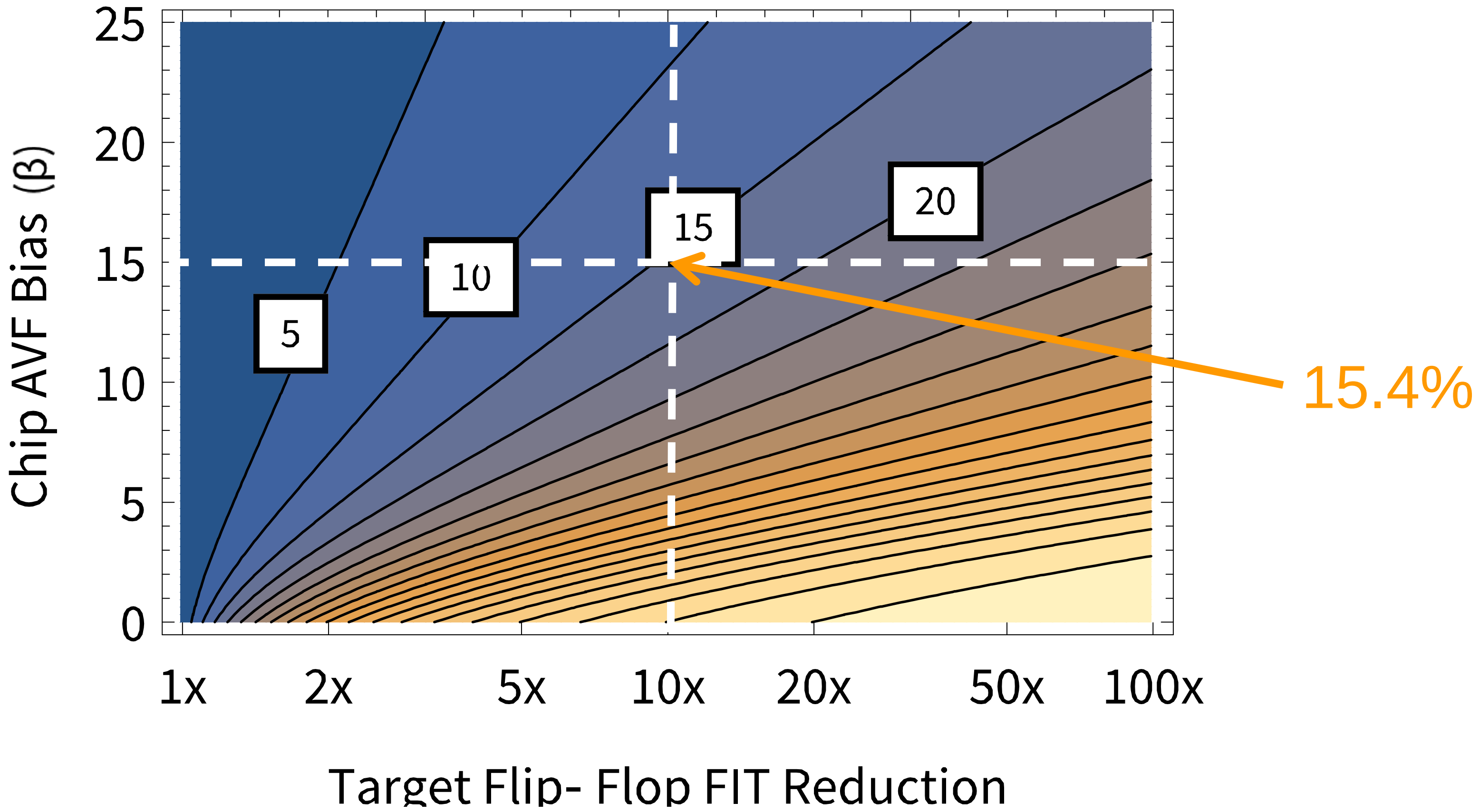
Hill 2008 FXP (β = 4.57):
60.5% FIT reduction

Uniform (β → 0):
20% FIT reduction

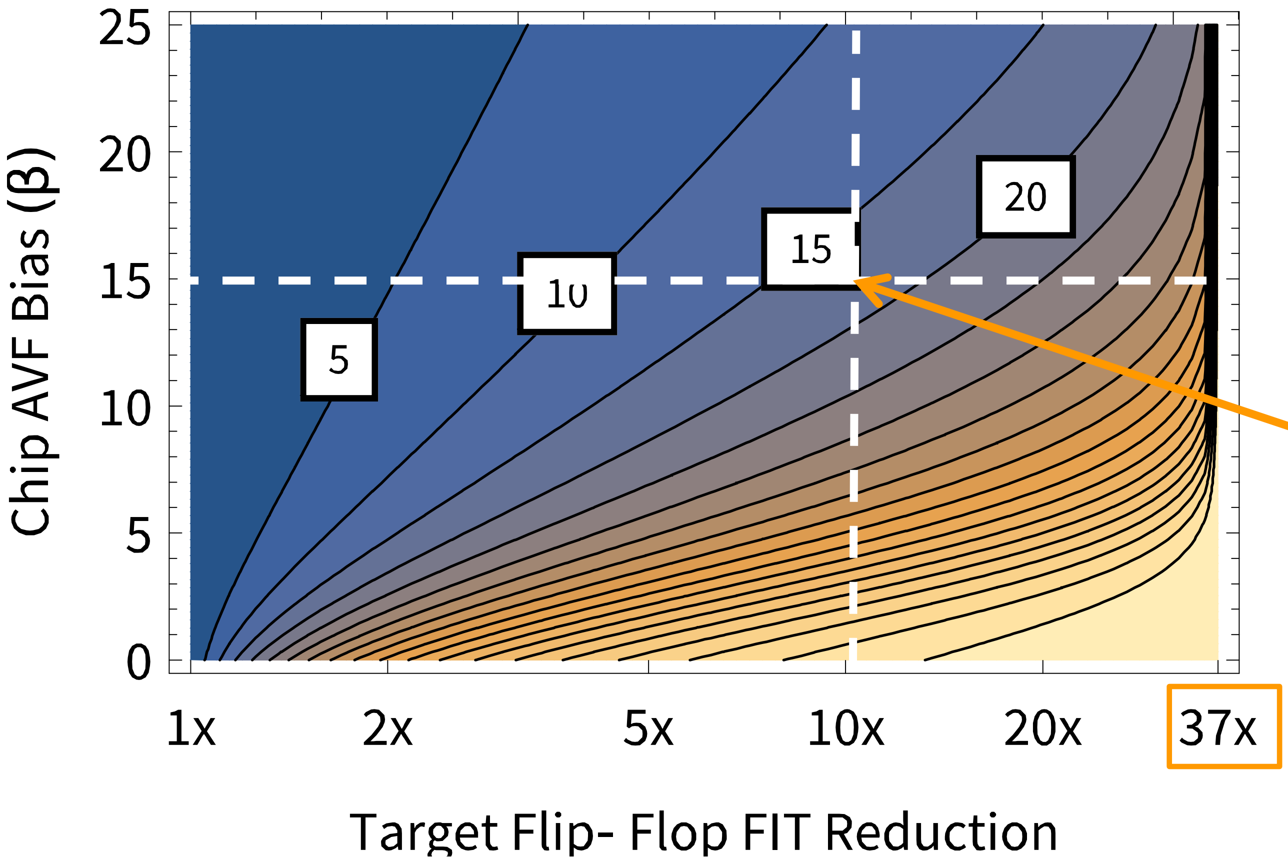
# DIFFERENT HARDENING LEVELS (β = 15)



# FRACTION OF FLIP-FLOPS THAT NEED BE HARDENED (TMR, β = 15)



# FRACTION OF FLIP-FLOPS THAT NEED BE HARDENED (REDUNDANT NODE, β = 15)

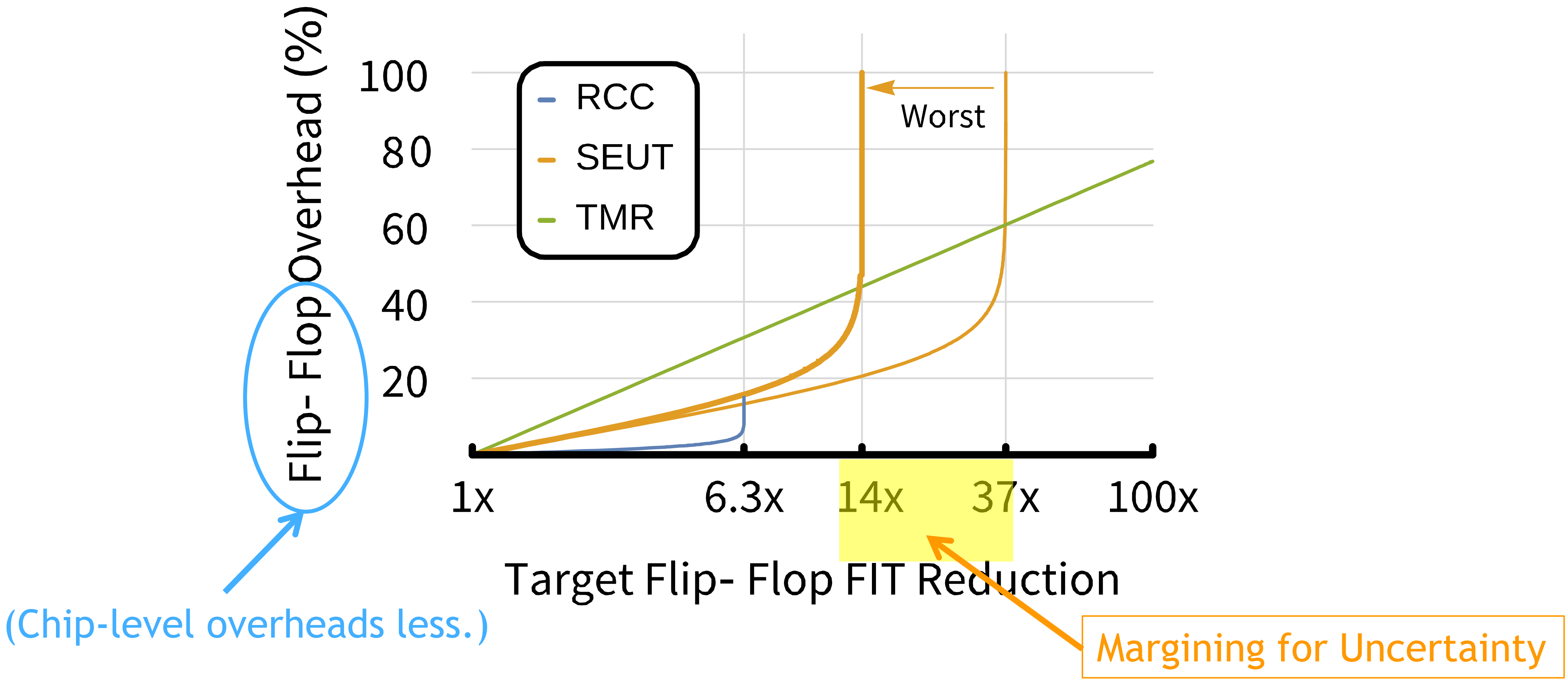



17.3%

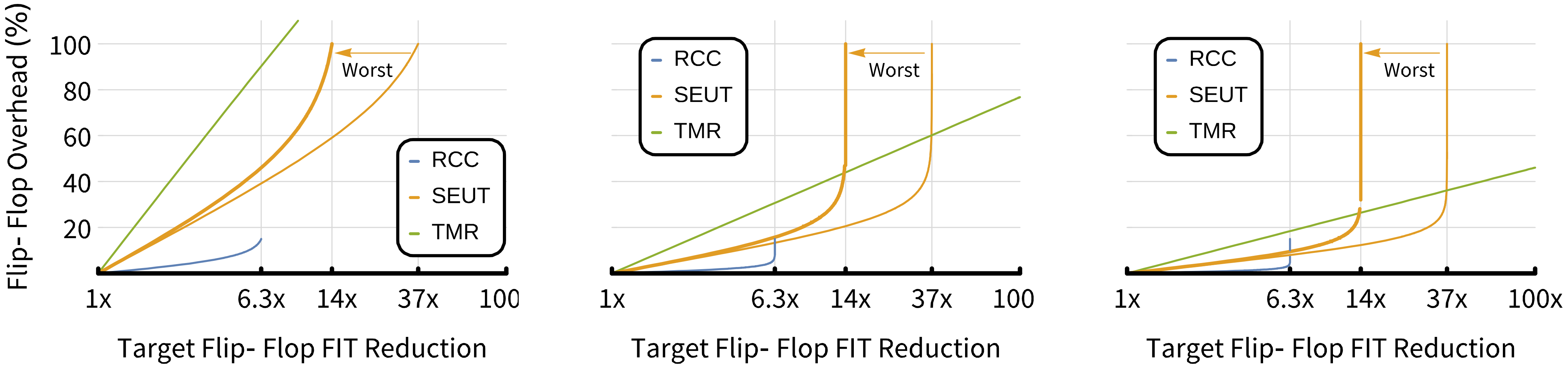
(vs TMR = 15.4%)

Max FIT Reduction

# COST DESIGN SPACE EXPLORATION (β= 15)



# COST DESIGN SPACE EXPLORATION

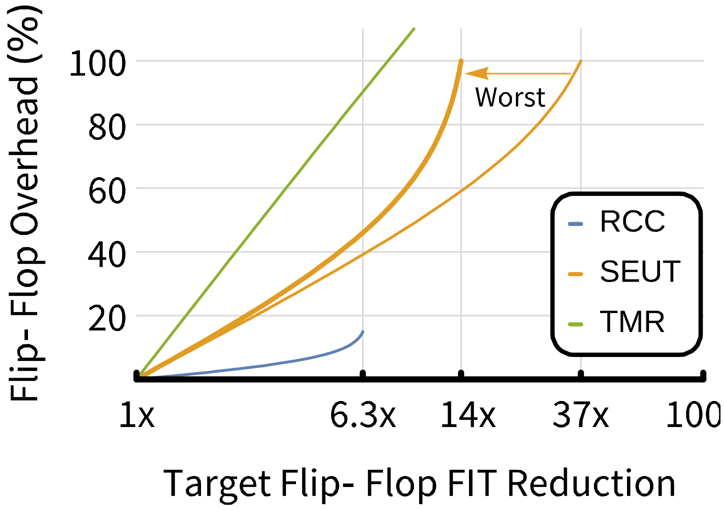



ß=5 (low bias)

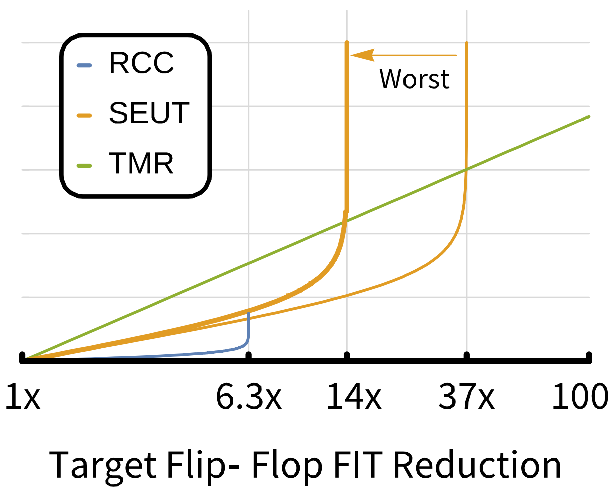
ß=15 (medium bias)

ß=15 (high bias)

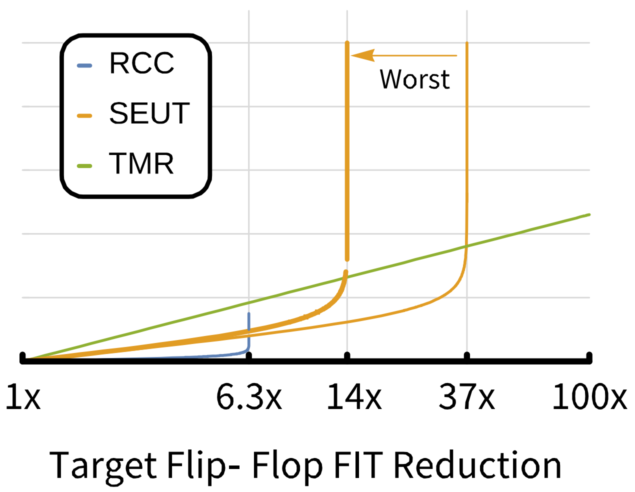
# COST DESIGN SPACE EXPLORATION




ß=5 (low bias)



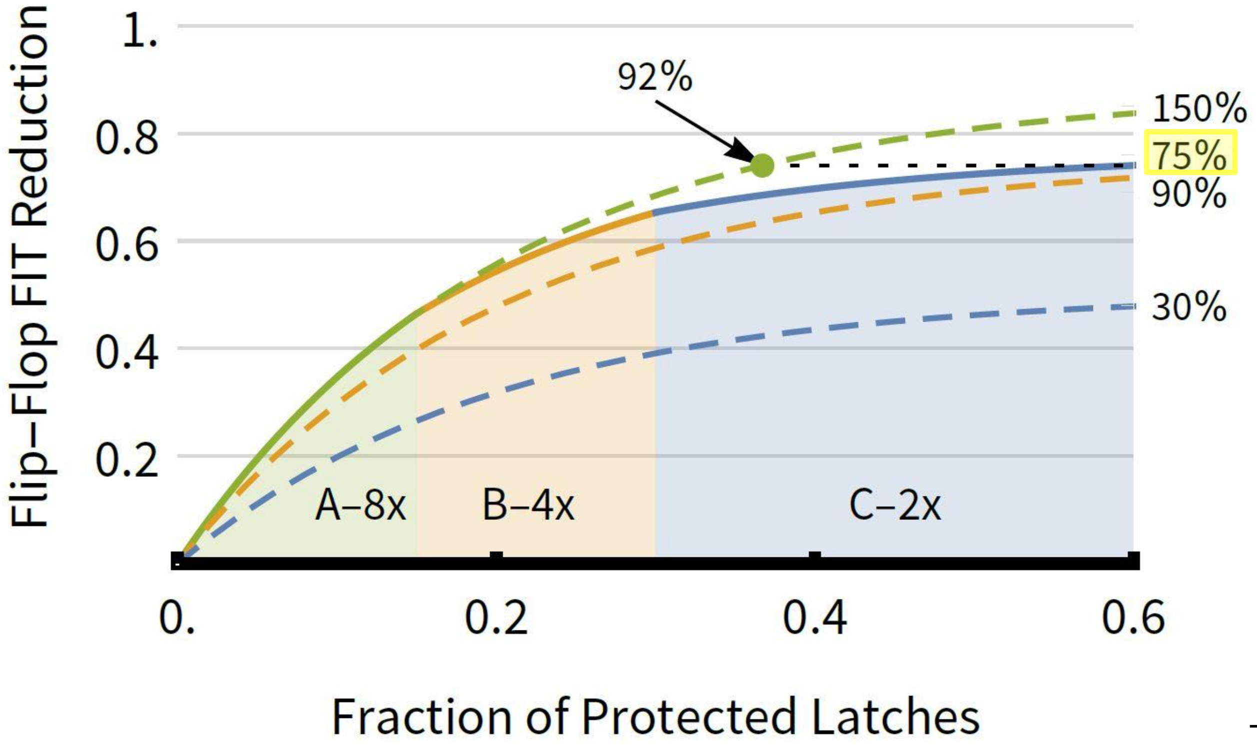

ß=15 (medium bias)




ß=25 (high bias)

Combinations of **multiple hardening techniques** also possible.

# MULTIPLE HARDENING EXAMPLE (β = 5)




A: 8x reduction, 3.5x overhead

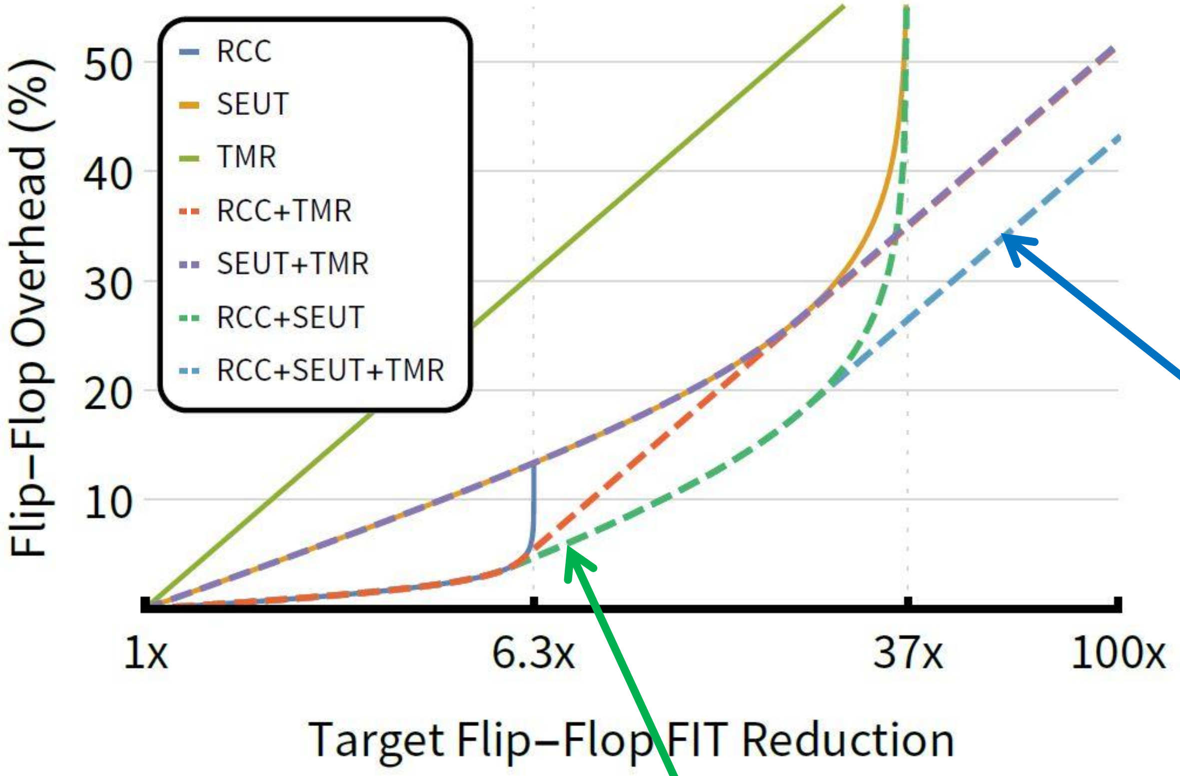
B: 4x reduction, 2.5x overhead

C: 2x reduction, 1.5x overhead

→ More efficient overall solution

→ More control over uncertainty

# MULTI-DESIGN SPACE EXPLORATION (β= 15)




RCC+SEUT+TMR
44% more efficient

RCC+SEUT 60% more efficient

# CONCLUSION

Some hardening of unstructured flip-flops is needed in the future

Not all flip-flops need be hardened—sensitivity is asymmetric

General: select the least costly design that hits the FIT target **with a healthy margin**

**Multi-hardening** promising:

- A rich design effort vs efficiency tradeoff space
- A possible way to control uncertainty